Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 10, with the following redlined paragraph:

During a set-up period of the crossbar matrix, the configuration is changed between B_1, and B_0. In configuration B_1, cells 12 sent from a port controller ~~1a~~25 are sent back to this respective port controller ~~1a~~25. During no-transmission time B_0, cells 12 sent from port controller ~~1a~~25 are not sent back to port controller ~~1a~~25. The inventive method works as follows.

Please replace the paragraph beginning at page 7, line 10, with the following redlined paragraph:

Fig. 3 depicts a port controller ~~1~~25 and a crossbar matrix 40. Port controller ~~1~~25 provides an input port 24, an output port 26, a cell memory 28, a start of cell signal generator 30, an offset counter 32, a serialiser 34, a de-serialiser 36 and a bit error indicator 38. Crossbar matrix 40 provides cell input ports ~~41~~41a-41n, cell output port ~~43~~43a-43n, switched connections 42 and interrupted connected 44. Further depicted is a central clock generator 48 and a configuration controller 46.

Please replace the paragraph beginning at page 7, line 16, with the following redlined paragraph:

Incoming packets at port 24 are segmented into fixed sizes packet fragments, cells, and stored in cell memory 28. Outgoing cells are reassembled back into packets and put out at port 26. During set-up of a port controller ~~1~~25, cells are sent at start of cell times which are generated at the start of cell time generator. These packets are serialised in serialiser 34 and sent to cell input port 41a. In loopback configuration, cell input port 41a is switched to cell output port 43a.

Please replace the paragraph beginning at page 7, line 31, with the following redlined paragraph:

During set-up the crossbar matrix 40 is switched between unit matrix and null matrix by configuration controller 46, which is controlled by a system clock signal generated by central clock generator 48. The system clock generated by central clock generator 48 is also

provided to offset counter 32 and to start of cell signal generator 30. Cells which are retransmitted to port controller ~~1~~ 25 are received in the serialiser 36. The received cells are evaluated in bit error rate indicator 38. In case a bit error occurred, the offset counter 32 is increased. By increasing the offset counter 32 the start of cell signal generator generates a start of cell time prevailing the central clock signal by the amount of the offset counter 32. By increasing the offset counter 32, the start of cell time will be changed until a cell is transmitted to crossbar matrix 40 and received by de-serialiser 36 without transmission errors, which means that the cell is received in crossbar matrix 40 in a transmission period.

Please replace the paragraph beginning at page 8, line 8, with the following redlined paragraph:

By applying the offset counter and the bit error indicator 38, start of cell times may be synchronised so as to align incoming cells at matrix 40 from various port controllers ~~1~~ 25.